WHAT IS CLAIMED IS:

1. A CPU, comprising:

a cache; and

control means,

wherein data are written into the cache and write back is performed to reflect the data written into the cache to an external memory at a desired timing,

the control means determining whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task, and then, when it is determined that the processing is possible, inhibiting access to the external memory.

2. The CPU according to claim 1,

wherein:

the control means detect free space in the cache and/or the amount of memory needed to process a task.

3. The CPU according to claim 2,

wherein:

in a situation where access to the external memory is inhibited, when the control means determine that the processing is impossible only with access to the cache, or when a cache miss occurs, the control means permit

access to the external memory.

4. The CPU according to claim 1, further comprising:

clock control means for controlling a clock frequency of an internal clock, the clock control means changing the clock frequency when access to the external memory is inhibited.

5. The CPU according to claim 1,

wherein:

the control means detect an address of a location where unnecessary data are stored in the cache and then free a cache space corresponding to the detected address.

6. The CPU according to claim 1,

wherein:

at an initial stage after power-on of the CPU, access to the external memory is inhibited after a program and data are loaded into the cache from the external memory.

7. The CPU according to claim 1,

wherein:

the control means determine whether or not access to the external memory is needed when a state of a task changes.

8. The CPU according to claim 1,

wherein:

the control means determine whether or not a program and data in the cache are purged, and then, if not purged, avoid loading the program and the data into the cache from the external memory.

9. An information processing device comprising:

a CPU which writes data into a cache provided therein and performs write back to reflect the written data into the cache to an external memory at a desired timing ;

the external memory; and

power supplying means for supplying power to the external memory,

the CPU including control means for determining whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task, and then, when it is determined that the processing is possible, inhibiting access to the external memory,

the power supplying means stopping power supply to the external memory when access to the external memory is inhibited.

10. The information processing device according to claim 9, the external memory includes a plurality of modules, and

the control means control power supply with respect to each of the modules.

11. A controlling method of a CPU which writes data into a cache included therein and performs write back to reflect the data written into the cache to an external memory at a desired timing,

the method comprising the steps of:

determining whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task; and

when it is determined that the processing is possible, inhibiting access to the external memory.

12. The method according to claim 11, further comprising the step of:

detecting free space in the cache and/or the amount of memory needed to process a task.

13. The method according to claim 12, further comprising the step of:

in a situation where access to the external memory is

inhibited, when it is determined that the processing is impossible only with access to the cache, or when a cache miss occurs, permitting access to the external memory.

14. The method according to claim 11, further comprising the step of:

when access to the external memory is inhibited, changing a clock frequency of an internal clock.

15. The method according to claim 11, further comprising the steps of:

detecting an address of a location where unnecessary data are stored in the cache; and

freeing a cache space corresponding to the detected address.

16. The method according to claim 11, further comprising the step of:

at an initial stage after power-on of the CPU, inhibiting access to the external memory after a program and data are loaded into the cache from the external memory.

17. The method according to claim 11, further comprising the step of:

determining whether or not access to the external memory is needed when a state of a task changes.

18. The method according to claim 11, further comprising the steps of:

determining whether or not a program and data in the cache are purged; and

if not purged, avoiding loading the program and the data into the cache from the external memory.